PATENT Attorney Docket No. 401572/SAKAI

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Shinya SOEDA

Application No. 10

10/077,767

Art Unit: 2811

Filed: February 20, 2002

Examiner: M. Prenty

For:

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE

SAME

## PENDING CLAIMS AFTER AMENDMENTS MADE IN RESPONSE TO OFFICE ACTION DATED NOVEMBER 22, 2002

- 1. A semiconductor device comprising:
- a semiconductor substrate having at least one DRAM region and one logic region; a resistor group including a plurality of resistors located in said logic region; a metal interconnection layer opposite said resistor grouping said logic region; and a metallic layer disposed between said resistor group and said metal interconnection

layer in said logic region as a shielding layer and partially disposed within said DRAM region.

- 2. The semiconductor device according to claim 1, wherein said metallic layer is a bit line layer in said DRAM region.
- 3. The semiconductor device according to claim 1, comprising a stacked capacitor in said DRAM region and including a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, said upper capacitor electrode layer being part of said metallic layer.
- 4. The semiconductor device according to claim 1, wherein said shielding layer has a fixed potential.
  - 5. A semiconductor device comprising:
  - a semiconductor substrate having at least one DRAM region and one logic region;
  - a signal interconnection layer in said logic region; and

In re Appln. of Shinya SOEDA Application No. 10/077,767

a metallic layer in said DRAM region and said logic region and located on one side of said signal interconnection layer, with respect to said semiconductor substrate, as a shielding layer in said logic region.

- 6. The semiconductor device according to claim 5, wherein said metallic layer is a gate electrode layer in said DRAM region.
- 7. The semiconductor device according to claim 5, wherein said metallic layer is a bit line layer in said DRAM region.
- 8. The semiconductor device according to claim 5, comprising stacked capacitor in said DRAM region and including a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, said upper capacitor electrode layer in said DRAM region being part of said metallic layer.
- 9. The semiconductor device according to claim 5, wherein said shielding layer has a fixed potential.
- 10. A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a metallic layer as a shielding layer in said logic region and in said DRAM region; and

forming a metal interconnection layer opposite a portion of said logic region where said resistor group is located.

- 11. The method according to claim 10, wherein said metallic layer is a bit line layer in said DRAM region.
- 12. The method according to claim 10, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer is part of said metallic layer.
  - 14. A method of fabricating a semiconductor device having at least one DRAM

In re Appln. of Shinya SOEDA Application No. 10/077,767

region and one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a first metallic layer as a first shielding layer in said logic region and in said DRAM region;

forming a signal interconnection layer in said logic region opposite said first shielding layer; and

forming a second metallic layer as a second shielding layer opposite said signal interconnection layer in said logic region and in said DRAM region.

- 15. The method according to claim 14, wherein one of said first and second metallic layers is a gate electrode layer in said DRAM region.
- 16. The method according to claim 14, wherein one of said first and second metallic layers is a bit line layer in said DRAM region.
- 17. The method according to claim 14, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer in said DRAM region is part of said second metallic layer.
- 18. The method according to claim 14, further comprising fixing potential of one of said first and second shielding layers.